Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A method for manufacturing a field effect transistor comprising:

providing an SOI substrate having a silicon layer formed on an insulating layer;

forming an active nitride film formed on the SOI substrate;

patterning the active nitride for form a mask;

forming a field oxide film for element isolation with the mask;

wet-etching the mask until the film thickness thereof is ~~reduce~~ reduced to allow an edge of the silicon layer contacting the field oxide film to be exposed;

implanting ions of a channel stopping impurity into the edge of the silicon layer by using the wet-etched mask; and

forming a gate electrode, a source and rain on the SOI substrate.

2. (previously presented) A method for manufacturing a filed effect transistor according to claim 1, comprising implanting ions of the channel stopping impurity vertically into the edge of the silicon layer.

3. (previously presented) A method for manufacturing a field effect transistor according to claim 1, comprising implanting ions of the channel stopping impurity at an angle into the edge of the silicon layer.

4. (previously presented) A method for manufacturing a field effect transistor according to claim 3, wherein the film thickness of the active nitride film is adjusted during the ion implantation in correspondence to the angle at which the ions are implanted.

5. (previously presented) A method for manufacturing a field effect transistor according to claim 1, further comprising:

implementing a heat treatment on the SOI substrate after implanting ions of the channel stopping impurity.

6. (previously presented) A method for manufacturing a field effect transistor according to claim 1, further comprising:

forming a sidewall constituted of the nitride film before forming the field oxide film for element isolation.

7. (previously presented) A method for manufacturing a field effect transistor according to claim 1, further comprising:

forming a silicon oxide film on an area where the edge of the silicon layer is exposed after wet-etching the mask.

8. (previously presented) A method for manufacturing a field effect transistor according to claim 1, further comprising:

forming a silicon oxide film on an area where the edge of the silicon layer is exposed after implanting the ions of said channel stopping impurity.

9. (previously presented) A method for manufacturing a field effect transistor according to claim 1, further comprising:

forming a sidewall constituted of a silicon oxide film at a side surface of the active nitride film after implanting the ions of said channel stopping impurity.

10. (previously presented) A method for manufacturing a field effect transistor according to claim 1, further comprising:

forming a sidewall constituted of a polysilicon film at a side surface of the active nitride film;

oxidizing the sidewall constituted of the polysilicon film after implanting the ions of said channel stopping impurity.

Claim 11-17 (cancelled).

18. (previously presented) A method for manufacturing a field effect transistor comprising:

providing an SOI substrate having a silicon layer formed on an insulating layer;

forming a gate electrode by etching a conductive layer formed on the silicon layer;

implanting ions to form a source and drain at an energy level at which all the impurity is injected into the silicon layer constituting the source and drain; and

implementing a heat treating at a low temperature under 950°C in order to activate the impurity at the source and drain;

wherein ions are implanted twice to form said source and drain, once at a low energy level achieving a high concentration and another time at a high energy level achieving a low concentration.

19. (previously amended) A method for manufacturing a field effect transistor comprising:

providing an SOI substrate having a silicon layer formed on an insulating layer;

forming a gate electrode by etching a conductive layer formed on the silicon layer;

implanting ions to form a source and drain at an energy level at which all the impurity is injected into the silicon layer constituting the source and drain; and

implementing a heat treatment at a low temperature under 950° C in order to activate the impurity at the source and drain;

wherein ions are implanted twice to form said source and drain, once at a low energy level achieving a high concentration and another time at a high energy level achieving a low concentration;

wherein the impurity concentration near the surface of said silicon layer is set equal to or higher than $10^{20}cm^{-3}$ through the ion implantation implemented at the low energy level achieving the high concentration with the impurity concentration becoming lower toward the rear surface of said silicon layer.

20. (previously presented) A method for manufacturing a field effect transistor comprising:

providing an SOI substrate having a silicon layer formed on an insulating layer;

forming a gate electrode by etching a conductive layer formed on the silicon layer;

implanting ions to form a source and rain at an energy level at which all the impurity is injected into the silicon layer constituting the source and rain; and

implementing a heat treatment at a low temperature under 950°C in order to activate the impurity at the source and drain;

wherein ions are implanted twice to form said source and drain, once at a low energy level achieving a high concentration and another time at a high energy level achieving a low concentration;

wherein the impurity concentration near the rear surface of said silicon layer is set higher than the channel concentration and equal to or lower than $10^{19}cm^{-3}$ through the ion implantation implemented at the high energy level achieving the low concentration.

21. (previously presented) A method for manufacturing a field effect transistor comprising:

providing an SOI substrate having a silicon layer formed on an insulating layer;

forming a gate electrode by etching a conductive layer formed on the silicon layer;

implanting ions to form a source and drain at an energy level at which all the impurity is injected into the silicon layer constituting the source and drain; and

implementing a heat treatment at a low temperature under 950°C in order to activate the impurity at the source and drain;

wherein ions are implanted twice to form a source and drain, once at a low energy level achieving a high concentration and another time a at high energy level achieving a low concentration;

wherein the impurity concentration near the rear surface of said silicon layer is set higher than the channel concentration and equal to or lower than $10^{19}cm^{-3}$ through the ion implantation implemented at the high energy level achieving the low concentration;

wherein the impurity concentration near the surface of said silicon layer is set equal to or higher than $10^{20}cm^{-3}$ through the ion implantation implemented at the low energy level achieving the high concentration with the impurity concentration becoming lower toward the rear surface of said silicon layer.